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DRAM MEMORY BASED DEEP DRIVEN ARCHITECTURE WITH REDUCED LOGICAL SPACE

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Abstract— Testing is the major bottleneck in all product development. The challenge of testing electronic systems to grow rapidly over the last decade. The complexity of large designs is increasing substantially, at the same time the technology feature sizes are decreasing. A circuit needs to be tested to conform the specifications. Testing of hardware is performed for two purposes to ensure the functionality and to ensure the absence of process faults. The first issue is primarily addressed through software simulation throughout the various iterations of the design. The second issue is most widely performed on large scale production testing. Built-In-Self test (BIST) is performed by employing a sample module, it is also known as Random Access Memory (RAM). The BIST RAM is taken into account under test and different advance test cases are given to check the circuit. The built-in-self test showing the logical compression is simulated in Modelsim software. This solution offers high memory capacity, increased bandwidth, fault tolerance and power characteristics needed for space missions.

Keywords— Built-in-self-test (BIST), fault tolerance, modelsim software, random access memory (RAM), testing.

I. INTRODUCTION

The increasing complexity of hardware design demands the methods for testing to follow the challenges that arise. The development in the test sector advances rapidly and provide solutions to fit new problems contribute to the new standards. Testing is not only a design verification, it is the purpose of testing to verify that the manufactured product is free of errors. BIST technology that improves aliasing, fault coverage and diagnostics as traditional BIST implementations produce pass/fail verdicts only and advanced BIST implementations produce more detailed diagnostic data as well, at the expense of additional silicon area. BIST tools are not integrated with a synthesis solution, which complicates the design flow, as a result of the random patterns, the fault coverage is hard to predict[1-4]. Solutions and methods that have improved BISTs efficiency with reasonable test patterns include test points, cellular automata implementations of the LFSR, weighting the bits produced by the LFSR and reseeding methods. A new approach that uses BIST for decompression / compression and is capable of applying deterministic patterns was introduced in. In this approach test patterns are encoded as seeds and applied externally.

Compared to traditional ATPG testing this method offers a significant reduction of test data volume and test application time[5-10].

The most widespread approach is test-per-scan BIST scheme. Unfortunately, many circuits contain random-pattern-resistant faults which limit the fault coverage that can be achieved with this approach. First method for improving the fault coverage for a test-per-scan BIST is to modify the CUT by either inserting test points or by redesigning it to improve the fault coverage. The drawback of these techniques is that they generally add additional logic levels to the circuitry that can degrade system performance. Fault coverage can be improved by another way by using weighted pseudorandom sequences. Additional logic is needed to weight the probability of each bit in the test sequence. The weight logic can be placed either at the input of the scan chain or in the individual scan cells themselves[11-17]. The disadvantage of the probability weighting approach is in the need of storing of the weight sets on chip and also, control logic is required to switch between weights, so the hardware overhead may be increased in size. A third method to improve the fault coverage is to use a "mixed mode" approach where deterministic patterns are used to detect the faults that the pseudorandom patterns miss. Storing deterministic patterns may require a large amount of hardware overhead. In a technique based on reseeding an LFSR was proposed that reduces the storage requirements[18-22].

II. RELATED WORK

MEDUSA is a predictable and high performance dram controller for multicore based embedded systems. In this method when processing write request, MEDUSA depends on FR-FCFS for high throughput and it immediately switch to read when read requests arrived at the reserved banks. A 3D DRAM based application specific hardware accelerator for SPMV, it implements an algorithm for large SPMV problems which make use of the underlying microarchitecture and overall system capabilities. This algorithm uses Variable Length Data Index (VLDI) technique to decrease the data transfer volume. Soft error study on DDR4 SDRAM using 480MeV proton beam is the study of logical upset in control logic. Soft error bits are affected by down scaling DDR technologies and it is compared with the retention weak bits. Bounding DRAM interference in COTS heterogeneous.[1-5]

MPSoCs for mixed criticality systems, a generalized interference delay analysis for DRAM main memory consider a breadth of features placed in COTS platform. Bringing 3D COTS DRAM memory cubes to space provides horizontal 3D stacking technology called Loaf-Of-Bread (LOB) combines multiple COTS DRAM memory dies into a cube design[6-9].

A COTS based novel 3D DRAM memory cube architecture for space applications is based on vertically combined by multiple COTS, 3D stacked, DRAM memory devices with radiation hardened by design (RHBD) controller. Memory access scheduler for efficient FR-FCFS scheduling exploits row-buffer locality by prioritizing the memory requests that access an already activated row. FR-FCFS reduces the average memory latency because row hit memory access reduces the latency of the activations. However, FR-FCFS causes unfairness on multi-core processors because it always prioritizes row-hit memory access.

To improve the fairness and the system throughput, the memory controller should prioritize the requests from a specified thread. Generally, the memory controller gives high priority to the request from a thread in the compute intensive phase, in which a thread issues few memory requests, because the progress per memory request from such thread is larger than that from the thread in the memory-intensive phase. However, it requires fine-grain detection of the execution phase transition to improve the performance because the phase frequently changes between the compute intensive and memory-intensive. The memory controller cannot give appropriate priority without the timeliness, which even worsen the

performance[10-14].

III. OVERVIEW OF DRAM

The memory consists of bits of data or program code arranged in a two-dimensional grid. DRAM memory stores bits of data called as storage or a memory cell, which are composed of a capacitor and a transistor. Storage cells are usually organized in a rectangular configuration. DRAM memory cells are dynamic, which means that they need to be refreshed every few milliseconds or given a new charge to compensate for the charge leakage of the capacitor. Modern DRAMs can be self-refreshed where no external logic is needed to instruct the DRAM and offer a row address[15-21]. In some cases, most of the data in DRAM can be recovered even if DRAM is not refreshed for several minutes. DRAM is a semiconductor memory option that system designers can use when building computers. Optional memory choices include static RAM (SRAM), electrically erasable replacement memory (EEPROM), NOR flash and NAND flash. Multiple systems use more than one type of memory.

A. Advanced Method

In this system a Built in self test is performed using a sample module which is nothing but a random access memory is designed. The BIST RAM is considered under test and differences advanced test cases are given to test the circuit, the performance is measure in such a way the power consumption reduction, Area efficiency is achieved. Bias variations a common problem in analog circuits and is getting worse as the technology scales. This is because the process variation is increasing and the power supply is reducing. With the increasing popularity of mixedsignal IC designs in the deep submicron processes, it is of interest to precisely measure analog voltages for test and debugging purposes. Such situations arise when measuring on-chip voltages for built-in self-test (BIST) .The analog voltages could be potentially located all over the chip. It is desirable that the measurement circuitry employed in such situations occupies as small an area as possible and is simple to design.

In this architecture, the dc voltages (of BIST sensors) of the test nodes are all tied together to a common bus and digitized centrally through ananalog-to-digital converter (ADC). Even ac signals are converted to dc through an envelope detector circuit, but calibration is required in this case to map the digitized values to analog amplitudes. In such cases, one has to know the number of sensor nodes in advance or design for a worst case scenario to ensure that the value on the bus settles within a specified time. Also, for the ac case, calibration puts a lower bound on the testing time required. It would be beneficial to have an approach where the design of a driver for the bus can be made independent of the number of test nodes, and also eliminate the need for calibration in testing A.C signals, which would reduce the time required for testing.

For the task of measuring analog voltages distributed all over the chip, the techniques described, require the analog signals themselves to be routed to the measuring unit. This is costly, as the analog signals will have to be shielded (to mitigate coupling), which can take up considerable area.

In our proposed approach, a small part of the measuring unit, called the sampling head (SpH), is placed at the measurement node itself, avoiding the routing of analog signals over long paths. The sampling head consists of a pair of delay cells and flip-flops, with certain control circuitry. The sampling head acts as a transducer which converts the analog voltage (to be measured) into the skew between a pair of subsampled signals. This clock pair is centrally processed in an all-digital manner to extract this skew.

B. Data Flow Analysis

Data Counter for memory Scheduler, Write / read buffering process is shown in fig.1. The data counter consists of clock, clear, count and blink. The data counter shows the flow of data

to perform read/write operation. Data analyzer is a process of transforming the useful information. Data analysis allow us to make informed decisions. Data analyzer consists of data distributor, analyzer and memory write shown in fig. 2. Data read operation transfers the desired word to address lines and activates the read control line. It is performed with line, memory read and memory write is shown in fig. 3.

ECG samples were added into clock line for processing the data. The main 3 leads data like P, Q and R data's in binary format were simulated. Integrating data into memory using port connections. It Reads the status of signal and ack signal exhaust strength from data and include it into main block.

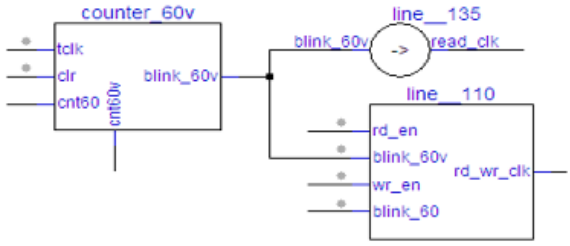
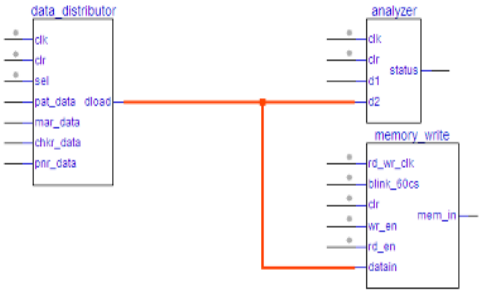


Fig. 1. Data flow of memory functions.



ig. 2. Data analyzer of data flow.

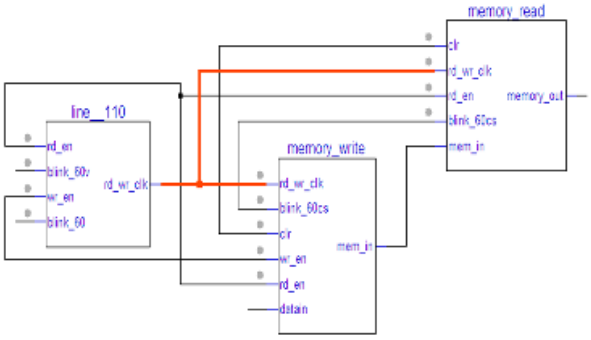


Fig. 3. Data read function.

C. *Testing Algorithm*

a) *Checker Board Test:* It is exactly sort of a chessboard which has alternate blocks of black and white, likewise, alternate values sequence like the "10101010101010101010" pattern is being loaded at high frequency and skim in high frequency. Just in case of any silicon, level fault exists in memory the results of this test turn positive indicating Fail.

b) *Marching Test:* It is nothing but the action of March fast. The info is being loaded into the memory forward direction like March fast, in regular intervals with reference to clock. The info is read from the memory and given for validation. Just in case of any silicon, a level fault exists in memory the results of this test turn positive indicating Fail.

c) *Pattern Test:* It is purely an optional test that's want to test the memory for silicon level issues by writing a hard and fast pattern of knowledge like "11001100" or "11111110" or "10100000" etc. this type is of operation helpful for the memory to

check if any logical mistakes exist in memory. Just in case of any silicon, a level fault exists in memory the results of this test turn positive indicating Fail.

d) Pseudorandom Test: Pseudo – Repeated Random – Undetermined Repeated random numbers are more accurate and specific when considering the testing of a tool. This type of knowledge is generated during a fixed interval at high frequency and loaded into the memory. Just in case of any silicon, a level fault exists in memory the results of this test turn positive indicating Fail.

IV RESULTS AND DISCUSSION

The system is designed by built-in test case which provides a design flow through XILINX ISE software to analyse the characteristics. The green colour waveform viewed in the simulation shows the flow of the memory module. The 8bit input is provided and the output is produced in the simulation result.

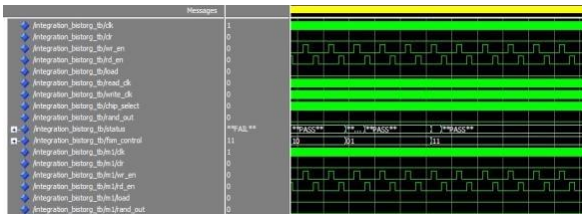


Fig. 4. Status of memory.

The status of memory shows whether the memory indicates pass or fail is shown in fig. 4.

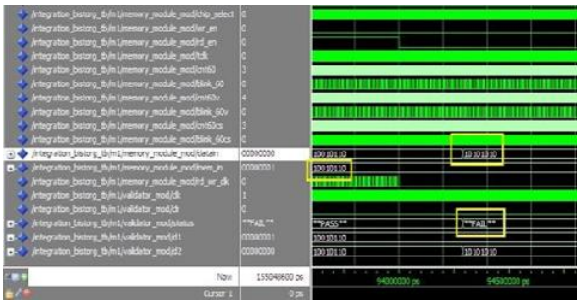


Fig. 5. Data in and memory in.

Waveforms for data in and memory in indicating that the memory fails when there is error in input is shown in fig. 5.

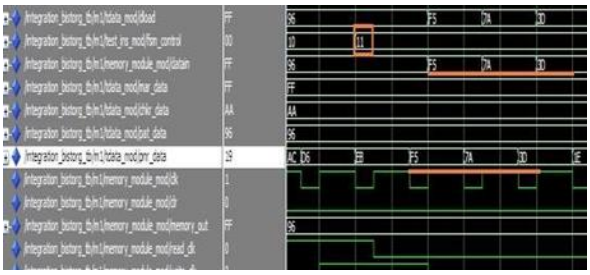


Fig. 6. Test bench result.

Simulation results with test bench shows the DRAM memory results using modelsim software is shown in fig. 6.

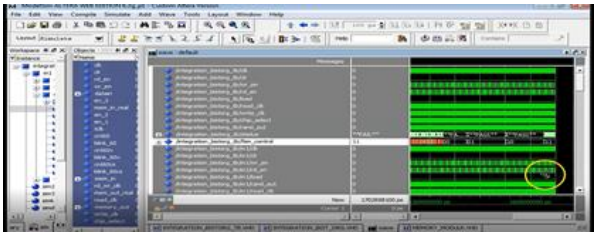


Fig. 7. FSM result.

The finite state machine shows the output logic with the mixture of both combinational and sequential logic. ECG noise signals were plotted in graph and memory architecture for ECG data were analyzed is shown in fig. 7.

V CONCLUSION

The prevailing system arrangement allows us to processing the data as fast than the other existing models. The overall output shows the increased efficiency. The design is done by the Xilinx software which gives the output waveform and the modelism shows the dataflow of the 3D-DRAM module. Using the LOB technology to stack COTS memory dies, the use of independent TSV dies and it achieve high memory capacity and good radiation tolerance. The controller is tested in hardware and a complete test board development is to subject the cube to radiation sources and the performances of the controller. The modular architecture allows flexibility in choosing memory die and the cube development design methodology is intended to be a building block which provides an additional opportunities such as integration of non-volatile memory or computing resources. In future another improved technique will be developed by using the multi-polynomial Linear Feedback Shift Register (LFSR) for encoding a group of deterministic test cubes. By using multi-polynomial Linear Feedback Shift Register (LFSR) technique in memory architecture would be more precise and versatile. The system on-chip replaces multi-chip design with equivalent functionality by reducing power consumption and semiconductor die.

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