Designing an effective Adiabatic Low Power CMOS Logic Circuit for energy efficiency using GDI technique

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ABSTRACT

When it comes to the electronics industry, power dissipation and circuit area are the most important considerations. According to previous research, the Full-Swing ADIABATIC GDI Technique has been shown to be an excellent way for low power digital design while also decreasing the circuit space. The proposed ALU architecture contains a 2x1 Multiplexer, 4x1 Multiplexer, and a low-power Full Adder cell for implementing arithmetic and logic operations. Cadence Virtuoso was used to simulate the 65nm TSMC process, which was completed successfully. When compared to earlier studies, the proposed design consumes less power and uses a smaller number of transistors while still attaining full swing function, according to the findings.

Keywords: GDI, Multiplier, multiplier register, arithmetic circuit, low power design

1.INTRODUCTION

Digital circuits, such as multipliers, are designed using circuit design principles, which are important considerations. First and foremost, in order to ensure that the multiplier operates at the desired clock rate, it is necessary for the designer to account both the critical path lag and the pipeline stage insert time. Second, alternative adder architectures are now being investigated in order to reduce the size of the multiplier. The circuit analysis technique assists the designer in ensuring that the adders in the design are both functional and perform as intended by the designer. The first order of business is to determine the architecture of the adder.. The speed of the adder can then be used to determine the number of pipeline stages to be used. If all of the requirements can be met, the size of the multiplier should be kept to a minimum as much as possible. Fast arithmetic necessitates the use of fast circuits. Fast circuits must be compact in order to minimize the delay effects of the wires in the circuit. In order to minimize wire delays, small size necessitates single-chip implementation. Furthermore, due to their small size, these fast circuits can be integrated as part of a larger single-chip system, allowing for even more input/output delay reductions. In order to address the growing need for low-power VLSI, it is important to create power-efficient logic types, among other things [1]. In the context of cell-based design, the performance criteria for logic styles include circuit speed, circuit size, power dissipation, wiring complexity, and the simplicity of use and generality of the gates employed in each logic style. Due to their high node activity and high clock loads, dynamic logic types are often a feasible option for high-speed circuit designs [2], but they are not ideal for low-power circuit implementations, which is a common misconception. For low-power applications, this chapter's purpose is to provide you an overview of several logic models. Because the size of various gadgets and devices is shrinking as a result of developments in manufacturing technology, we must reduce the number of CMOS logic cells in order to keep up with technological advancement. In terms of energy efficiency, asymmetrical logic circuits (ALCs) are one of the most effective technologies now in use. The ECRL, 2N-2N2P, and PFAL are among the adiabatic logic families examined in this research. Every run of the simulation was done with the W/L ratio of each circuit held constant to enable a consistent comparison of results. HSPICE's average power dissipation characteristics were displayed on a graph, which was then used to compare the power dissipation characteristics of other logic families. Advanced Materials released the results of applying the HSPICE algorithm in 65nm technology with a supply voltage of 1V and a frequency of 100MHz.

2.LITERATURE SURVEY

CMOS LOGIC STRUCTURE:

As of today, complementary metal oxide semiconductors (CMOS) are the dominant technology in the semiconductor industry. The CMOS technology is used to implement the vast majority of high-speed microprocessors. Today's CMOS technology is characterized by the following characteristics: Despite the fact that the connection limits the amount of area available, small minimum-size transistors allow for dense architectures. Quiescent Power is another exceedingly low feature of current CMOS technology. The alternating current (AC) power generated by capacitance charging and discharging during the operation of classic CMOS circuits has a substantial impact on their power consumption:

$\text{Power}=CV^2f$ Equation (1)

There are two variables in this equation: The frequency at which the capacitance is charged or discharged, and C. As the circuits become faster, the frequency increases, which in turn increases the power consumption? The fabrication process is relatively straightforward. Transistors with large widths are required in order to drive wires quickly, as large voltage swings (typically 3.3 to 5 volts) are experienced in contemporary CMOS (with even smaller swings on the way). In the

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absence of additional variables, Equation (1) indicates that a smaller voltage swing will occur quicker than a larger voltage swing. The figure shows a CMOS inverter with a large noise margin and low power consumption. When it comes to transistors, you may choose between two basic designs: pull-up PMOS and pull-down NMOS. The output will be independent of the size relationship between the pull-up and pull-down transistors while the circuit is in steady state. This reduces the need for pass-transistor logic systems to be concerned about signal degradation, which is a benefit of CMOS complementary logic systems. It uses almost no static power during the transition because the power-to-ground path is only closed for a brief period of time.

PASS TRANSISTOR LOGIC

NMOS or PMOS transistors are used to develop a design in the pass transistor logic [3] style, depending on the application. It demonstrates how an XNOR can be implemented using pass-transistor logic. This circuit employs signals A and B as controllers and pass signals, respectively. When A is true in this circuit, the value of B is passed to the output. It is passed the complement of A if the condition A is false. Because they are not always active, logic forms that are not always active have a limited ability to be used in extended chains of logic like the example above. Complicated Boolean functions may be implemented in significantly less physical area because to the smaller form factor of pass-transistor logic. To implement CMOS complementary logic, the XNOR needs three two-input NAND gates with twelve transistors each. Pass-transistor logic only necessitates the use of two transistors. Due to the limited voltage swing, the output voltage swing in CMOS logic is greater than that in pass transistor logic, despite the fact that there are less transistors in pass transistor logic.

TRANSMISSION GATE LOGIC

For complementary switching or transmission, we go into detail into the connections between transistors. n- and p-channel transistors, each with its own gate connection and shared source and drain connections, make up this circuit. FIGURE 1 illustrates the application of a control signal S to the gate of an n-device and its inverse to the gate of a p-device. This is best understood by viewing the n and p devices in isolation, as shown in Figure 1. The n and p devices are turned off when the control signal S is set to zero. A high output impedance is the consequence. When S is high, i.e. 1, input is transferred to the output node and vice versa since it activates both the n and p devices.

3. EXISTING METHOD

A sub-threshold Adiabatic Logic solution for ultralow-power applications is presented by Manash Chanda and colleagues. The author of this work aims to develop Ultra Low-Power applications by investigating the performance of logic circuits that operate in the sub-threshold area. By constructing and simulating a four-bit CLA, we have shown that subthreshold [5] adiabatic logic is very effective. To reduce the peak power dissipation of a multiplexer, SonalAron and colleagues devise a technique [6]. As a result of using the PFAL adiabatic approach, the peak power dissipation of the multiplexer is reduced by 29.876 microwatts. In reality, for low-power applications, this reduction in power dissipation can be quite helpful. M1 Sowmiya (Eastern Time). PFAL adiabatic logic circuits are used in the fundamental gates that have been presented. For ultralow power applications, the author found that the suggested adiabatic logic circuit is favourable since the NOT gate, NOR gate, and NAND gate achieved power savings of 23%, 36.1 %, and 42.8 percent when compared to typical CMOS logic gates utilising Tanner EDA. Another benefit of employing a NAND gate over the other two gates is that it consumes less electricity. This demonstrates that adiabatic logic-based NAND gates with positive feedback can be employed in ultra-low-power circuitry. An ET is Vijendra Pratap Singh. The downsides of PFAL were extensively examined. Although the typical static PFAL provides greater power performance, the adiabatic PFAL is not suited in instances where delay is a primary concern owing to a lengthy switching time or low speed operation. The character V. S. is a fictitious one. In his essay, Kanchana Bhaaskaran proposes the Energy Recovery Performance of Quasi-Adiabatic Circuits [9], which he describes in detail. As a result of the use of Lower Technology Nodes, the author examines the modelling and efficiency analysis of sense-amplifier based quasi-adiabatic topologies such 2N-2P and 2N-2N2P circuits [10]. Pre-resolving capacity of DCPAL's pre-resolving capability is explained in detail, including the impact of circuit construction on the adiabatic frequency range, current leakage channels, and floating nodes.

4.PROPOSED SYSTEM

Unique circuits for the XOR/XNOR functions, as well as the XOR–XNOR functions that are executed simultaneously, are proposed in this paper. Due to their low output capacitance and low short-circuit power dissipation, the circuits under study are very well optimised in terms of power consumption and delay. These full-adder (FA) circuits are all based on our XOR–xNOR (XOR/XNOR) gates that swing fully in both directions. For example, each of the circuits has considerable benefits over the others in terms of sped-up performance and other characteristics. Comprehensive simulations using HSPICE and Cadence Virtuoso are used to assess the overall performance of the designs that are presented. It was shown that employing a 65-nm CMOS process model, the proposed designs outperform previous FA systems in both speed and power consumption. Circuits' power dissipation performance is improved using a novel transistor size method. It is suggested that the goal value for optimum PDP be achieved with the fewest iterations possible [11] using a particle swarm optimization algorithm. Supply and threshold voltages, output capacitance, input noise immunity as well as transistor size are all examined.

ARITHMETIC LOGIC UNIT

To design the ALU, the Full-Swing ADIABATIC GDI approach is utilised, with the following steps:

A. 2x1Multiplexer

Figure 1 shows a multiplexer, which is a digital switch that uses a select signal [4] to pick the output from various inputs. Six transistors are used in a 2x1 multiplexer.

B. 4x1Multiplexer

16 transistors are all that is needed to build a 4 x 1 multiplexer like the one depicted in Fig. 2.

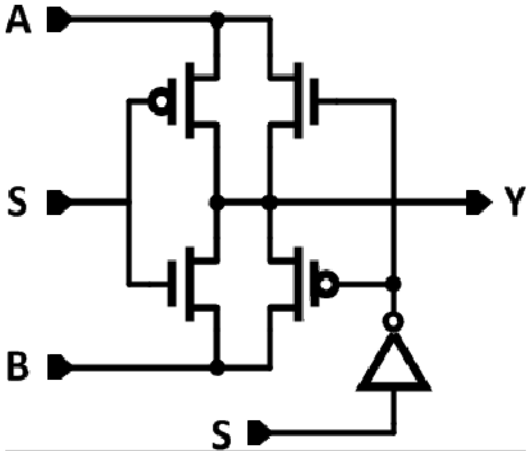

Fig.1.Full-Swing ADIABATICGDI2x1 Multiplexer

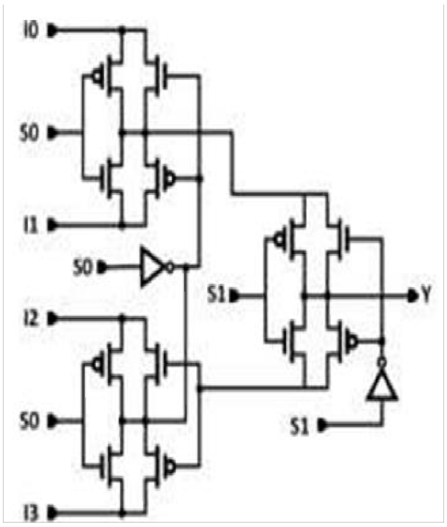

Fig.2.Full-Swing ADIABATICGDI4x1 Multiplexer

C. Full Adder

Three input bits must be added together in order to build a complete adder, which is a combinational circuit. Figure 3 depicts the system's inputs and outputs for your convenience. Full-swing AND, OR, and XOR gates were used to create the adder cell in this design. Among three alternatives, this design was chosen because it consumes the least amount of power, has the shortest latency [12], and can perform logic operations on par with the ALU.

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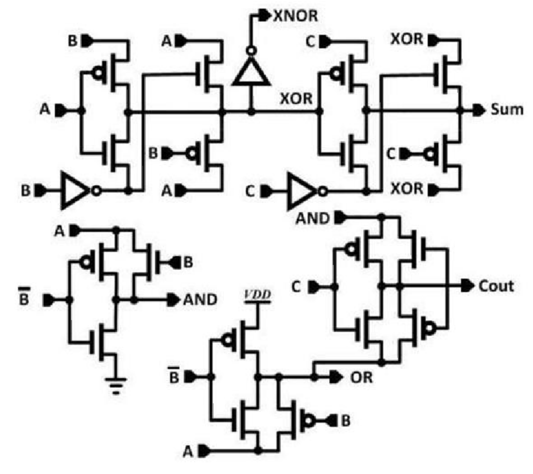

Fig.3. Full-Swing Full Addercell

D. Design of the Arithmetic Logic Unit

Even the smallest microprocessors feature an arithmetic logic unit (ALU), which is a critical component of the Central Processing Unit (CPU). Addition, subtraction, incrementing / reducing / increasing, as well as logic operations like AND, OR, XOR, and XNOR [6,] and other operations, are all accomplished. Using the circuits previously described, the 4-bit ALU is proposed to have an architecture consisting of four stages, each of which is a 1-bit ALU: According to Fig. 4, which depicts the architecture of a 1-Bit ALU stage, each stage needs 48 transistors due to the inclusion of two 2x1, two 4x1, and one complete adder cell. Using the selection line S0, S1, and S2 codes as a starting point, any procedure can be carried out. In Table I, the proposed ALU's truth table is shown.

“Table.1. Truth table of the proposed 4 Bit ALU”

S2	S1	S0	Operations
0	0	0	Decrement
0	0	1	Addition
0	1	0	Subtraction
0	1	1	Increment
1	0	0	AND
1	0	1	XOR
1	1	0	XNOR
1	1	1	OR

B input 4x1 multiplexer chooses from logic 1, B - 0 and logic 1 for Decrement, Addition, Subtraction and Increment operations depending on the values of S0 and S1 selection lines. S2 selects between arithmetic and logic operations based on the values of the S0 and S1 selection lines.

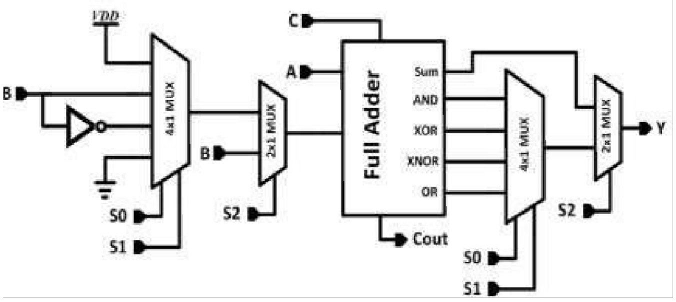

Fig.5.Schematic of 1-Bit ALU Stage

The 4-Bit ALU seen in Figure 5 was built using four processes. None of the other values have any bearing on logic 1's findings whatsoever. In order to get logic 1, which is necessary for subtraction and increment operations, the carry input of ALU0 is attached to selection line S1. However, the other values have no influence on the logic operations conducted on logic 1.

5.SIMULATION RESULTS AND DISCUSSION

To enhance power and delay performance while preserving low power consumption, 65nm TSM-CMOS technology was used to build four-bit ALU circuits using PMOS transistors that were three times bigger than NMOS transistors.

One volt of energy powered the Cadence Virtuoso simulator, which was used to run the simulations. In terms of power consumption and transistor count, the suggested ALU architecture outperforms the competition. The proposed ALU consumes electricity at or below the bare minimal levels set by the manufacturer. When compared to other designs, the number of transistors in this model is also less than in the other designs.

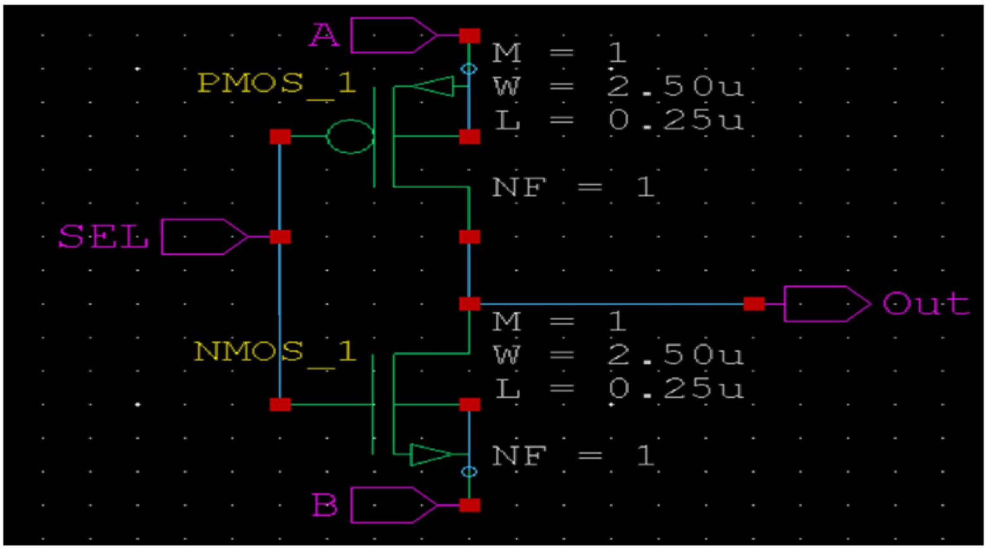

Fig.6. Proposed 2to1 Mux

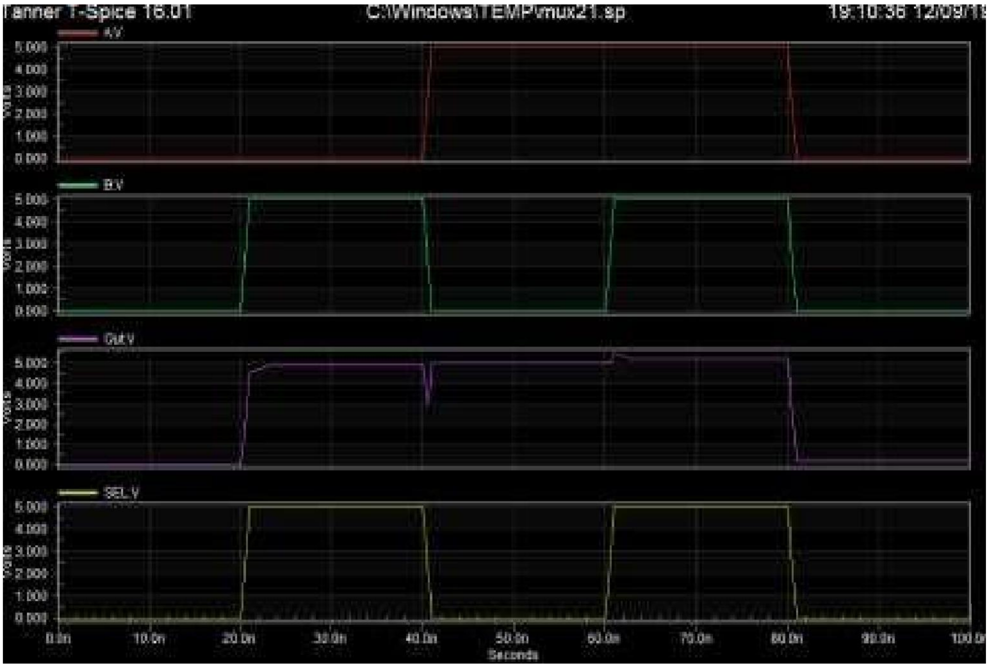

Fig.7. Proposed 2 to1 MUX output

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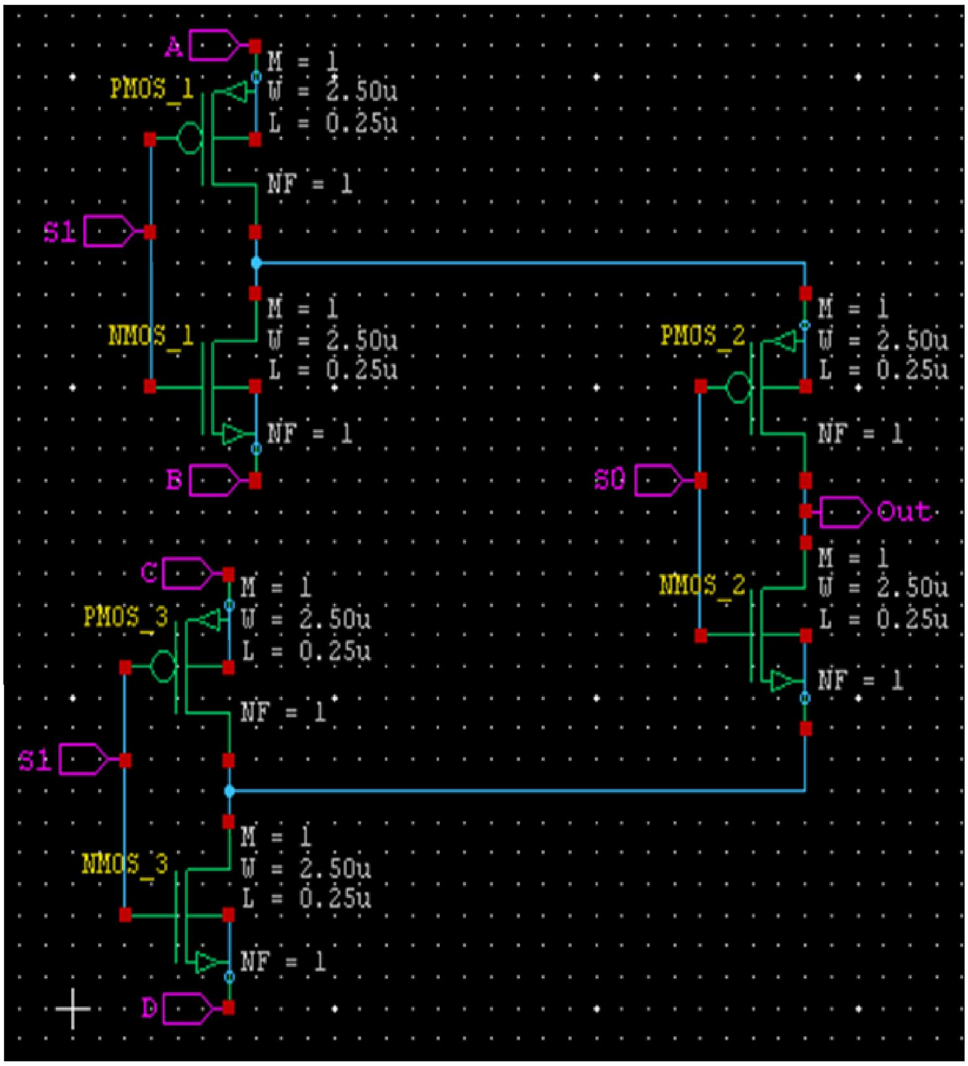

Fig.8. Proposed 4 to1 Mux

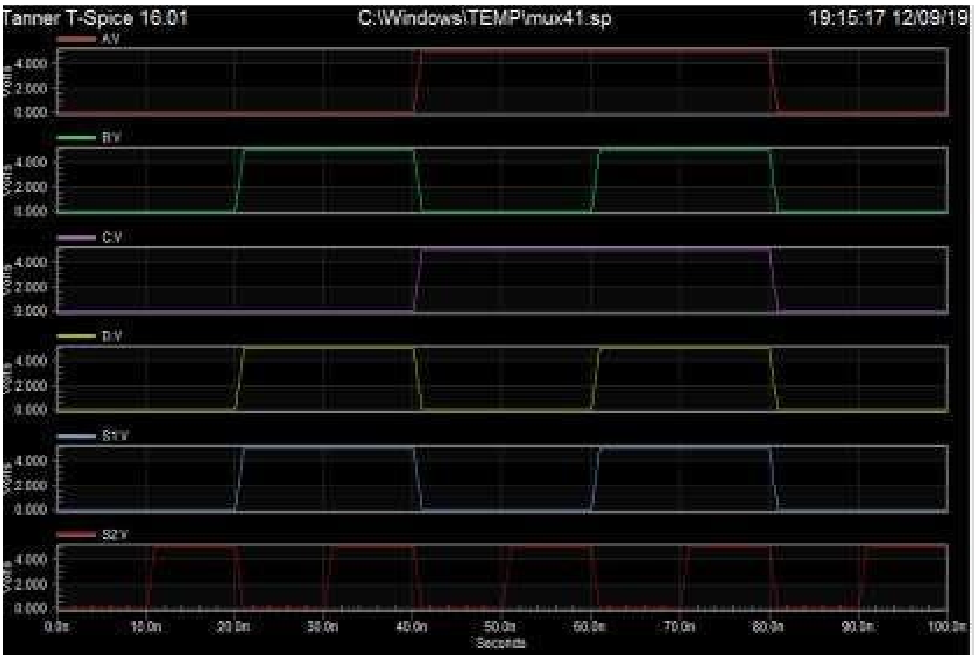

Fig.9. Proposed 4 to1 Mux output

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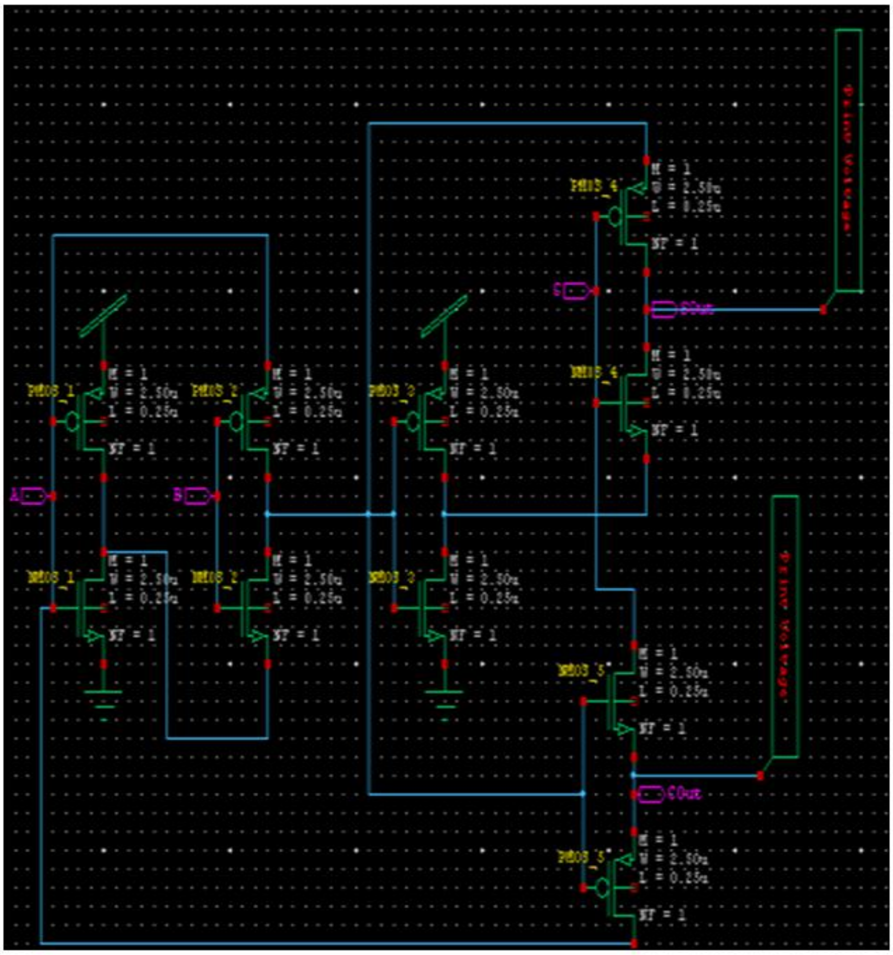

Fig.10. Proposed Full Adder

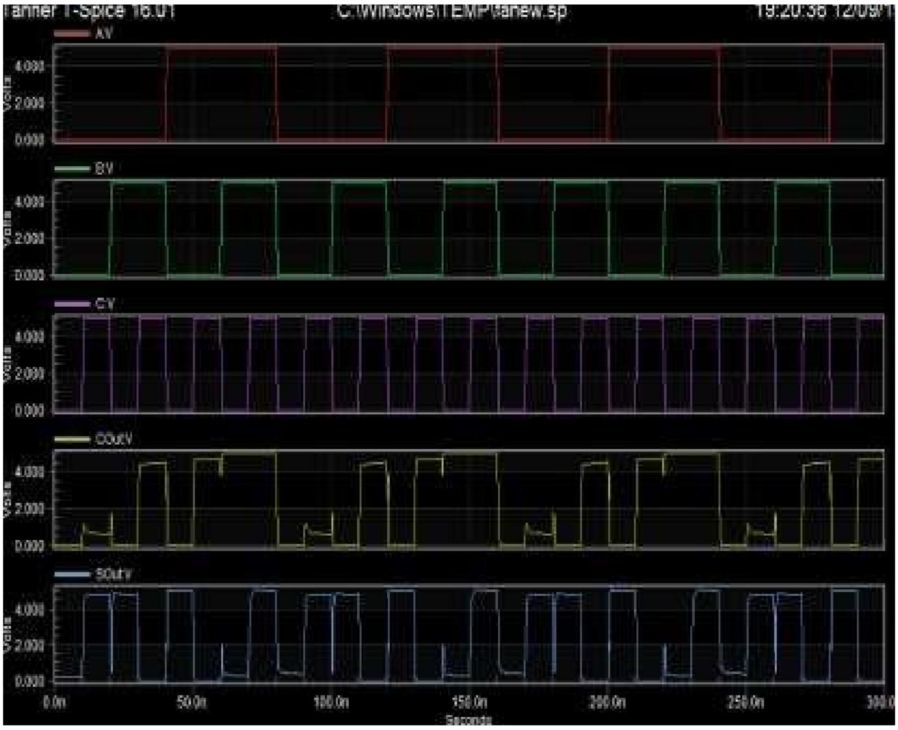

Fig.11. Proposed Full Adder Output

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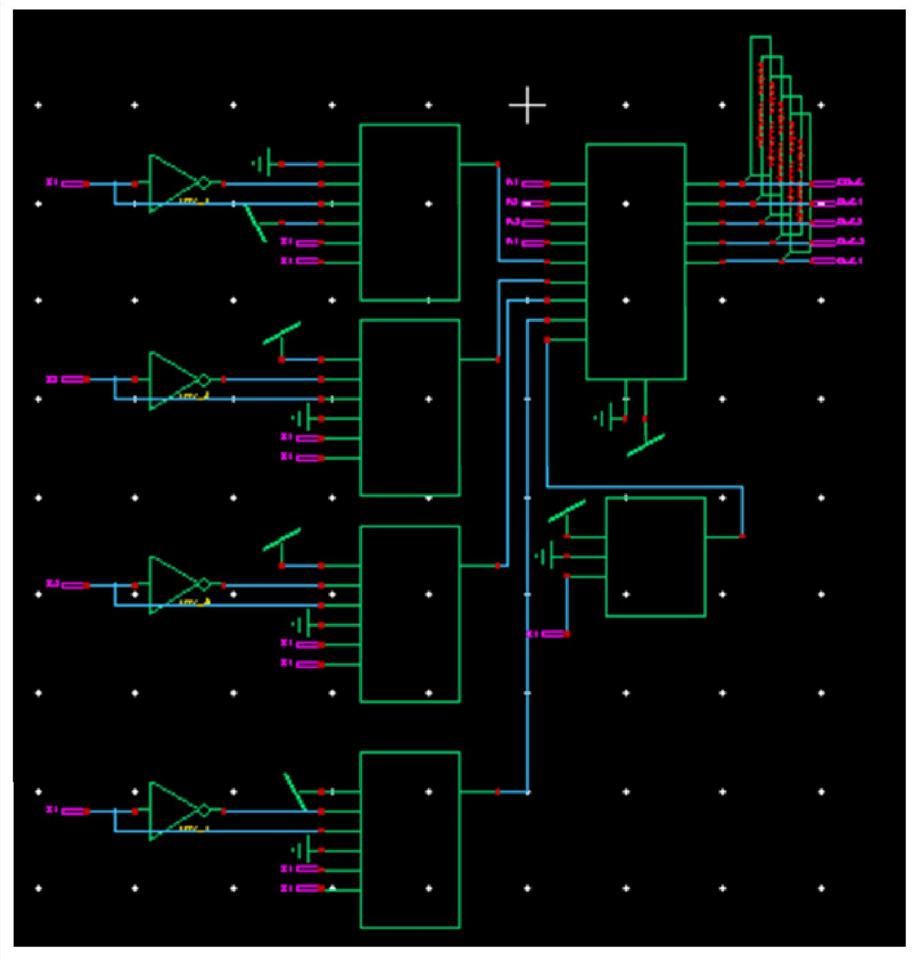

Fig.12. Proposed Arithmetic Unit

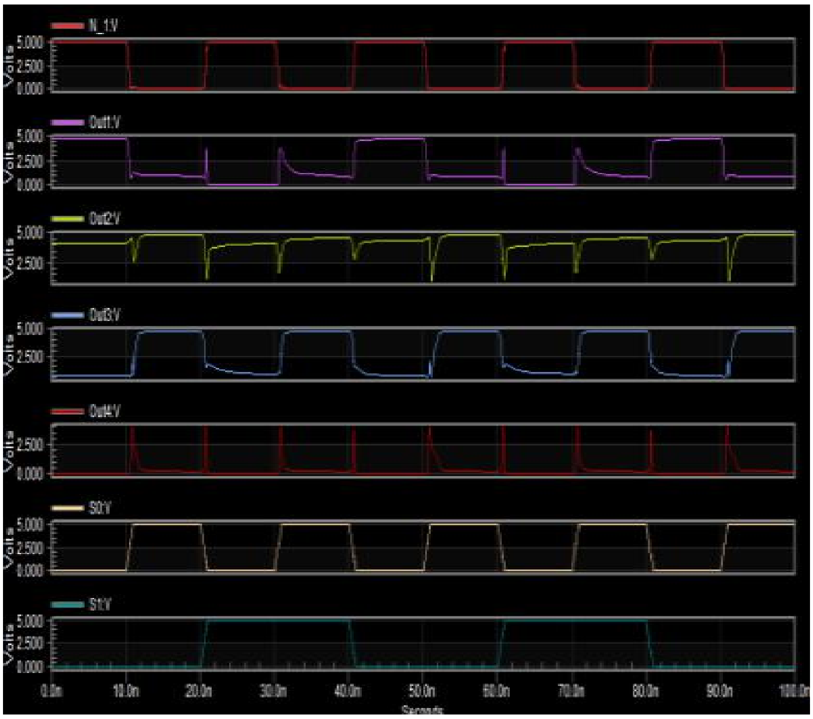

Fig.13. Proposed Arithmetic Unit Output

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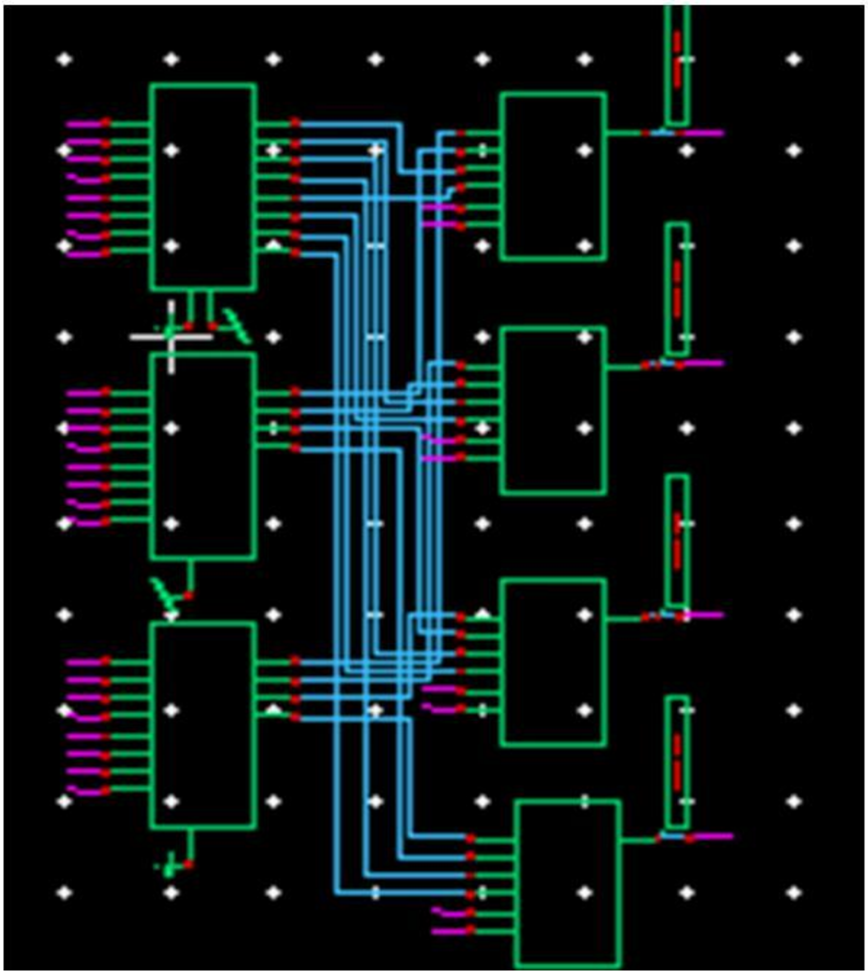

Fig.14. Proposed Logic Unit

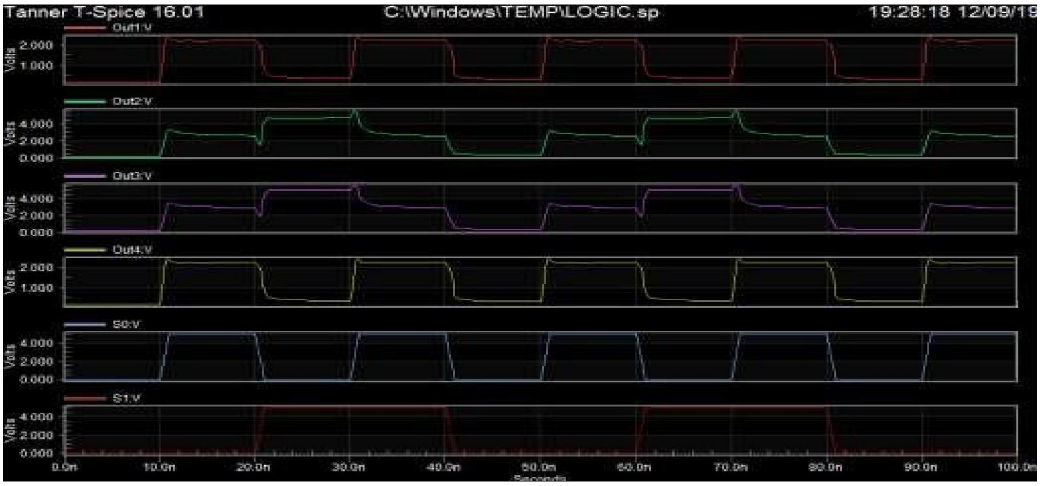

Fig.15. Proposed Logic Unit Output

Power consumption in modern electronics is becoming a rising source of worry as the desire for longer battery life, lower heat dissipation, and greater device reliability continues to climb. GDI approach is used to construct a 4-bit Arithmetic and logic unit in this work, which demonstrates how power optimization may be achieved at the architecture level. The less the number of transistors, the smaller the surface area of silicon that is required for the circuit to function. This design shows that in terms of performance characteristics, it performs better than the prior design.

6.CONCLUSION

Using the Full-Swing ADIABATIC GDI method and Cadence's Virtuoso simulator, this study shows how a 4-Bit ALU can be built in the 65nm CMOS process of TSMC and then emulated. It was found that despite maintaining Full-Swing Operation, the suggested ALU architecture was more power efficient and had a lower transistor count. The proposed design utilises 138 transistors and runs on a 1V supply voltage. The system works as described.

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